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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,490	12/04/2003	Zi-Ping Chen	681954.0046	7535

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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,490	CHEN ET AL.	
	Examiner	Art Unit	
	SCOTT BAUER	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,16,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,16,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 22 recites the limitations "the p-type and n-type transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. The p-type and n-type transistor limitation was removed in the amendment of claim 16.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 20010007521) in view of Su et al. (US 6,590,261).

With regard to claim 1, Chen in Fig. 13C teaches an integrated circuit for electrostatic discharge (ESD) protection (paragraph 0008) comprising: a silicon-controlled rectifier (comprising intrinsic BJT's npn & pnp) including a first transistor (46, 72 & 78) integrally formed with the SCR, wherein the first transistor has a first gate (72) located over a channel between a first doped region (46) of the SCR and a second doped region (78) of the SCR; a contact pad (40) coupled to the SCR.

Chen does not teach a control circuit coupled to the silicon-controlled rectifier, wherein the control circuit changes a normal holding voltage of the SCR to a modified holding voltage to keep the SCR in latch-up after detecting a electronic static discharge event, and changes the modified holding voltage of the SCR to the normal holding voltage after a time period to keep the SCR from latching up; and wherein the first gate of the first transistor is not directly coupled to the control circuit.

Su, in Figure 4, teaches an SCR used for ESD protection similar in structure to the ESD protection SCR's found in Figs. 13 A & 13C. Su further teaches a control circuit (222) coupled to the silicon-controlled rectifier, wherein the control circuit changes a normal holding voltage of the SCR to a modified holding voltage to keep the SCR in latch-up after detecting a electronic static discharge event, and changes the modified holding voltage of the SCR to the normal holding voltage after a time period to keep the SCR from latching up; and wherein the control circuit is coupled to the P doped region (210) to control the holding voltage of the SCR (column 4 lines 25-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen with Su, by coupling the control circuit of Su to the P doped region (78) of the SCR of Chen, for the purpose of preventing the SCR from being triggered improperly and causing damage to the ESD device (Su column 2 lines 55-57).

If the control circuit of Su is connected to the SCR of Chen , the gate of Chen would not be directly coupled to the gate as it would be coupled to the doped region (78) instead.

With regard to claims 2-5, Chen in view of SU discloses the device of claim 1. Su further discloses that the control circuit further comprising an output terminal coupled to the first and second gates (re claim 2), wherein the control circuit further comprising a resistor, a capacitor and an output terminal disposed between the resistor and the capacitor (re claim 3), the control circuit including a resistor-capacitor delay circuit (re claim 4). Chen further teaching that the SCR further comprising a p-type substrate (42), an n-well (n-well) formed in the p-type substrate, a p-type diffused region (46) formed in the n-well, and an n-type diffused region (48) formed outside of the n-well.

3. Claims 16, 21 & 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. In view of Lai et al. as applied to claims 1, 8 & 23 above, and further in view of Tong et al. (US 6,756,834).

With regard to claim 16, Lee teaches an integrated circuit comprising: a contact pad (Vin); a first silicon-controlled rectifier (35 & 36), the first SCR associated with the contact pad, wherein the first SCR includes first MOS transistor (25, 26 & 38) integrally formed with the SCR; wherein for the first SCR, a gate (38) of the first MOS transistor is coupled to the contact pad or ground.

Lee does not teach a control circuit, wherein a control circuit is coupled to the first SCR, wherein the control circuit changes a normal holding voltage of the SCR to a modified holding voltage to keep the SCR in latch-up after detecting an electrostatic

discharge event, and changing the modified holding voltage of the SCR to a normal holding voltage after a time period to keep the SCR from latching up or that the circuit provides a plurality of contact pads, a plurality of control circuits or that there is a plurality of SCRs.

Lai teaches an SCR used for ESD protection similar in structure to the ESD protection SCR's found in Figs. 13 A & 13C. Lai further teaches a control circuit coupled to the silicon-controlled rectifier, wherein the control circuit changes a normal holding voltage of the SCR to a modified holding voltage to keep the SCR in latch-up after detecting a electronic static discharge event, and changes the modified holding voltage of the SCR to the normal holding voltage after a time period to keep the SCR from latching up; and wherein the control circuit is coupled to the P doped region to control the holding voltage of the SCR.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

Tong et al., in figure 1, discloses an ESD protection circuit comprising a plurality of pads, first and second voltage sources of first and second voltage levels, and a plurality of ESD protection circuits (10 & 14). Tong et al. further teaches that each ESD protection device contains a control circuit comprising a capacitor (16) and a resistor (18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Lee with Tong et al. by protecting a plurality of I/O pads and voltage lines with the SCR device taught by Lee for the purpose of providing ESD protection to an entire chip assembly instead of just a single voltage source.

With regard to claims 21 & 22, Lee in view of Lai and Tong discloses the device of claim 16. Lai further discloses that the control circuit further comprising a resistor-capacitor delay circuit (re claim 21), and Lee in view of Lai further teaches that the control circuit further comprising an output terminal coupled to a gate of each of the p-type and n-type transistors.

Response to Arguments

Applicant's amendment of claim 1 to include that the control circuit is not coupled to the gate necessitated the new grounds rejection of claims 1-5. The amendment of claim 16 does not include this limitation, and dependant claim 22 states that the control circuit output is coupled to the gates of the SCR and as thus the newly amended claim is still unpatentable of Lee in view of Lai and Tong.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT BAUER whose telephone number is (571)272-5986. The examiner can normally be reached on M-F 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

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